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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/703,034	10/31/2000	Joseph R. Zbiciak	TI-30553	8913

23494 7590 09/02/2010

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EXAMINER	
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ART UNIT	PAPER NUMBER
2193	

NOTIFICATION DATE	DELIVERY MODE
09/02/2010	ELECTRONIC

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JOSEPH R. ZBICIAK

Appeal 2009-003141
Application 09/703,034[1]
Technology Center 2100

Before JOSEPH L. DIXON, THU A. DANG, and
CAROLYN D. THOMAS, *Administrative Patent Judges*.

THOMAS, *Administrative Patent Judge*.

DECISION ON APPEAL[2]

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[1] Application filed October 31, 2000. The real party in interest is Texas Instruments Incorporated.

[2] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, or for filing a request for rehearing, as recited in 37 C.F.R. § 41.52, begins to run from the "MAIL DATE" (paper delivery mode) or the "NOTIFICATION DATE" (electronic delivery mode) shown on the PTOL-90A cover letter attached to this decision.

STATEMENT OF THE CASE

Appellant seeks our review under 35 U.S.C. § 134 of the Examiner's final decision rejecting claims 13 and 25-29, which are all the claims remaining in the application, as claims 1-12 and 14-24 are cancelled. We have jurisdiction over the appeal under 35 U.S.C. § 6(b).

We AFFIRM-IN-PART.

The present invention relates to microprocessors optimized for digital signal processing. (Spec., 1, l. 26.)

Claim 13 is illustrative:

> 13. A digital system having a microprocessor operable to execute a rounding dot product instruction, wherein the microprocessor comprises:
>
> storage circuitry for holding pairs of elements;
>
> a multiply circuit connected to receive a first number of pairs of elements from the storage circuitry in a first execution phase of the microprocessor responsive to the dot product instruction, the multiply circuit comprising a plurality of multipliers equal to the first number of pairs of elements;
>
> an adder/subtractor circuit having a plurality of inputs each connected to received a corresponding one of the plurality of products from the plurality of multipliers and a mid-position carry input to a predetermined bit for mid-position rounding responsive to the rounding dot product instruction; and
>
> a shifter connected to receive an output of the adder/subtractor circuit, the shifter operable to shift a selected amount in response to the rounding dot product instructions.

Appellant appeals the following rejections:[3]

1. Claim 28 under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which Appellant regards as the invention;

2. Claim 13 under 35 U.S.C. § 103(a) as being unpatentable over Saishi (US 6,167,419, Dec. 26, 2000) and Pitsianis (US Patent Pub. 2003/0088601, May 8, 2003); and

3. Claims 25-27 under 35 U.S.C. § 103(a) as being unpatentable over Saishi and Peleg (US 6,385,634 B1, May 7, 2002).

FACTUAL FINDINGS

Saishi

1a. Saishi discloses that a "multiplicand is multiplied by a multiplier using a multiplication process, the result of the multiplication is added by an addition process to a rounding signal to be output from a rounding signal generation process. . . . By carrying out a rounding process in the addition process by using the rounding signal . . ." (Abstract.)

1b. Saishi discloses in Figures 1-5 a rounding signal (106, 206, 315, 415, and 515) being inputted into an addition means. (Figs. 1-5.)

1c. Saishi's Fig. 8 discloses a predetermined rounding position in element 811. (Fig. 8.)

[3] The Examiner withdrew the rejection of claims 13 and 25-29 under 35 U.S.C. § 101 (Ans. 12-13).

ANALYSIS

35 U.S.C. § 112, second paragraph Rejection
Claim 28

Regarding the § 112, 2nd paragraph rejection, Appellant argues claim 28 separately (App. Br. 7). *See* 37 C.F.R. § 41.37(c)(1)(vii). *See also In re Young,* 927 F.2d 588, 590 (Fed. Cir. 1991).

The Examiner found that the "shifting" limitations in claim 28 are unclear and incomplete (Ans. 4). We disagree.

The test for definiteness under 35 U.S.C. § 112, second paragraph is whether "those skilled in the art would understand what is claimed when the claim is read in light of the specification." *Orthokinetics, Inc., v. Safety Travel Chairs,* 806 F.2d 1565, 1576 (Fed. Cir. 1986)(citations omitted).

Claim 28 recites, *inter alia,* "shifting said first product an instruction specified number of bits . . ." The Specification discloses that the "[s]hifter 440 provides a fixed value shift of either zero bits or sixteen bits." (Spec., 23, ll. 8-9.) We find that in light of the Specification, one skilled in the art would understand what is being claimed in the shifting limitation, i.e., a shift of a fixed value.

Therefore, we reverse the Examiner's § 112, second paragraph rejection of claim 28.

35 U.S.C. § 103(a) rejection over Saishi and Pitsianis
Claim 13

Appellant separately argues claim 13. *See* 37 C.F.R. § 41.37(c)(1)(vii). *See also In re Young,* 927 F.2d 588, 590 (Fed. Cir. 1991).

Appellant contends that "both Saishi et al and Pitsianis et al teach rounding in a portion of the circuit different from that recited in claim 13." (App. Br. 16.)

Issue: Did the Examiner err in finding that the combined teachings of Saishi and Pitsianis disclose "an adder/subtractor circuit having a plurality of inputs each connected to receive a corresponding one of the plurality of products from the plurality of multipliers and a mid-position carry input to a predetermined bit for mid-position rounding"?

The Examiner found that Saishi's Figures 1-5 discloses that "the multiplication means is not a multiplier only but the multiplication means composes the multiplication stage and the addition stage." (Ans. 14.) The Examiner further found that "[t]he missing feature/limitation in the primary reference by Saishi et al., 'the dot product instruction for multiplying multiple pairs of elements', is clearly found in the secondary reference by Pitsianis et al., particularly Figures 3B and 6." (Ans. 15.) We agree with the Examiner.

Saishi discloses a multiplication method that uses multipliers, addition means, and a rounding signal (FF 1a). Saishi further discloses that the rounding signal is inputted at the addition means and goes to a predetermined rounding position (FF 1b-1c). Appellant has not shown how Saishi's predetermined rounding process is distinguishable from the claimed "predetermined bit for mid-position rounding." Thus, we find that Saishi discloses the argued mid-position rounding signal being inputted into the addition means, consistent with the claimed invention.

Therefore, Appellant has not shown that the Examiner erred in rejecting claim 13. Accordingly, we affirm the rejection of claim 13.

35 U.S.C. § 103(a) rejection over Saishi and Peleg
Claims 25-27

Appellant argues claims 25-29 as a group (App. Br. 18-23). For claims 26 and 27, Appellant repeats the same argument made for claim 25. We will, therefore, treat claims 26 and 27 as standing or falling with claim 25.

Appellant contends that "Peleg et al fails to teach any circuit in Figure 8 for rounding." (App. Br. 20.) Appellant further contends that "Saishi et al never states that the rounding signal is input to 'a mid-position carry input to a predetermined bit' as recited in claim 25." (App. Br. 21.)

Issue: Did the Examiner err in finding that the combination of Saishi and Peleg discloses "an adder/subtractor circuit having . . . a mid-position carry input to a predetermined bit?"

The Examiner found that "any Figures 1-5 within the cited reference by Saishi et al. disclose the above alleged limitations, particularly Figure 5." (Ans. 18.) We agree.

As noted *supra,* Saishi discloses an adder receiving as an input a rounding signal to a predetermined bit (FF 1a-1c). Appellant has not shown how Saishi's predetermined bit is distinguishable from the claimed "predetermined bit." Thus, we are not persuaded of error.

Based on the record before us, we find that the Examiner did not err in rejecting claims 25-27. Accordingly, we affirm the rejections of claims 25-27.

DECISION

We reverse the Examiner's § 112, second paragraph, rejection of claim 28; and

We affirm the Examiner's § 103(a) rejections of claims 13 and 25-27.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a). *See* 37 C.F.R. § 1.136(a)(1)(iv) (2010).

AFFIRMED-IN-PART

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